

ISSN No. (Print) : 0975-8364 ISSN No. (Online) : 2249-3255

Simulation and Analysis of Carbon Nanotube Based cum CMOS based Folded cascode Op Amp

Bal Krishan*, Sanjai Kumar Agarwal^{*}, Sanjeev Kumar^{**} ^{*}YMCA University of Science & Technology, Faridabad, (HR), INDIA ^{**}Noble Group of Institutions, Junagadh (Gujarat), INDIA

(Corresponding author: Bal Krishan) (Received 04 February, 2015 Accepted 26 March, 2015) (Published by Research Trend, Website: www.researchtrend.net)

ABSTRACT: In this research paper, Simulation and Analysis of innovative folded cascode Operational Amplifier based on carbon nanotubes (CNT) has been performed using 45 nm technology. DC voltage gain, average power, bandwidth and output resistance have been computed. CNT based folded cascode Op Amp results in high performance with the increase of CNTs. For example, the increase in DC gain is 41.48% in pCNT based folded cascode Operational Amplifier and 13.93% in nCNT based folded cascode Operational Amplifier; decrease in average power is by 16.86% in pCNT based Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS based folded cascode Operational Amplifier in comparison to CMOS based FC-OP AMP in comparison to conventional CMOS based Folded Cascode OP AMP. The low output resistance has resulted in a small bandwidth in CNT based FC-OP AMP.

Further, the simulation studies have revealed that the performance of the CNT based folded cascode Op Amp can be improved optimized at different CNTs.

Keywords: CNTs, folded cascode Op Amp, simulation, dc gain, power consumption, output resistance, Bandwidth.

I. INTRODUCTION

As CMOS technologies evolves well into short channel length, the supply voltage decreases and device characteristics deteriorate. These conditions pose severe challenges in Op Amp designs. The transistor intrinsic gain becomes low due to inferior device output impedance [1-5].Now in order to ensure further improvement in FET performance with sustaining Moore's Law, it is necessary to look for alternative like Carbon Nanotube Field Effect Transistors (CNFETs) that promise to deliver much better performance than existing MOSFETs. CNFET technology can also be easily clubbed with the bulk CMOS technology on a single chip and utilizes the same infrastructure [4]. There has been a lot of work available in the literature on the digital applications of CNFET but its analog applications have not been explored [5,6]. Keeping the foregoing in mind, this paper investigates in detail the performance of Pure CNFET Folded cascode Op

Amp at 45nm for obtaining high gain, low power consumption, and low output resistance etc. In this work, we simulated two CNT based FC-OP AMPs and compared the performance with the conventional CNT based FC-OP AMP, uses N CNTFETs as sinks and conventional PMOS transistor as sources. It is being called as pCNT based folded cascode Operational Amplifier. Similarly, another proposed CNT based COTA uses P CNTFETs as sources and conventional NMOS transistors as sinks and is being called as nCNT based folded cascode Operational Amplifier. Simulation and analysis of innovative folded cascode Op Amp based on carbon nanotubes (CNT) has been performed using 45 nm technology node. The simulation is being done by using HSPICE. The comparative analysis of the proposed CNT-FC-OP AMP with the conventional CMOS based Folded Cascode OP AMP has shown the increase in DC gain of around 41.48% in pCNT based folded cascode Operational Amplifier and around 13.93% in nCNT based folded cascode Operational Amplifier.

Further decrease in average power is by 16.86% in pCNT based folded cascode Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS-FC-OP AMP respectively. However, the output resistance has decreased in CNT based FC-OP AMP in comparison to conventional CMOS based Folded Cascode OP AMP. The low output resistance has resulted in a small bandwidth in CNT based FC-OP AMP. Further, the simulation studies have revealed that the performance of the CNT based folded cascode Op Amp can be improved optimized at different CNTs.

This paper begins with an overview of Carbon Nanotube Field Effect Transistors (CNFET) and Folded cascode Op Amp in Section 2. Section 3 covers the design of pure CNFET Based Folded cascode Op Amp. Section 4 gives conclusion.

II. CARBON NANOTUBE AND CARBON NANOTUBE FIELD EFFECT TRANSISTOR

In 1991 Iijima observed concentrically nested carbon structures while investigating the soot of an arcdischarge experiment between two graphite electrodes. These structures were multiwalled carbon nanotubes (MWCNTs). After two years, Iijima and Ichihashi of NEC [10] and Bethune and colleagues of the IBM Almaden Research Center in California [11] discovered single-walled carbon nanotubes (SWNTs). These are allotrope of carbon. CNT is being considered as a promising and is being projected to replace the widely used silicon. It has remarkable properties, like high tensile strength more than steel, electrical conductivity more than the best conductor silver, thermal conductivity more than diamond. The semiconductor industry is facing some major challenges at the nanoscale dimension. Such problems include power and performance optimization, device fabrication and control of process variations at nanoscale and integration of a diverse set of materials and devices on the same chip [8]-[9]. A single walled carbon nanotube (SWCNT) is a one-dimensional conductor, that can be either metallic or semiconducting depending upon the arrangement of carbon atoms decided by their Chirality, Ch (i.e. the direction in which the graphene sheet is rolled) whose magnitude and relationship with CNT diameter is given by Eqs. (1) and (2) respectively where 'a' is the grapheme lattice constant (0.249nm) and n1, n2 are positive integers that specify the chirality of the tube.

$$C_{h} = a \quad (n^{2}_{1} + n^{2}_{2} + n_{1} n_{2}) \qquad \dots (1)$$

$$D_{CNT} = C_{h} / \qquad \dots (2)$$

A compact model for single-walled CNTFETs was proposed [4]-[5]. This CNTFET model can be simulated in HSPICE [5].



(a) SWCNT

(b) MWCNTs

Fig. 1. Different types of Carbon NanoTubes.



Fig. 2. Different types of SWCNTs.



Fig. 3. Three Dimensional CNTFET structure.

III. PROPOSED CNTFET BASED FOLDED CASCODE OP AMP DESIGN

The Fig. 4 shows the schematic of a folded-folded cascode op-amp using a class AB output buffer. In the frequency response of the op-amp, the load of the op-amp is a 1 pF capacitor. Folded cascode Operational transconductance is designed at different carbon nanotubes (N). The widths of CNTFET and MOSFET are chosen to be identical for a reasonable comparison.

We simulated two CNT based FC-OP AMPs and compared the performance with the conventional. Fig. 4 shows the circuit diagram of one of the proposed CNT based FC-OP AMP. It uses N CNTFETs as sinks and conventional PMOS transistor as sources. It is being called as pCNT based folded cascode Operational Amplifier. Similarly, another proposed CNT based COTA uses P CNTFETs as sources and conventional NMOS transistors as sinks and is being called as pCNT based Operational Amplifier.

A. Variation of CNTs (N)

The current drive in a CNTFET depends both on the number of CNTs per device ('N') and thus DC Gain increases with CNTs as shown in figure 5. In addition, current driving capability of CNTFET goes up with the large number of tubes which reduces the output resistance as shown in figure 6, thereby allowing greater fan-out .The bandwidth increase with CNTs since output resistance decreases as shown in figure 7, Also, the average power increases but it is still very small as shown in Fig 8.



Fig. 4. Proposed PMOS-NCNT-FC-OP-AMP.







Fig. 6. Variation of CNTs for Output resistance.



Fig. 7. Variation of CNTs for 3dB Bandwidth.



Fig. 8. Variation of CNTs for Average Power.

Table 1	1:	Technology	Parameters	of	CNFET.
---------	----	------------	-------------------	----	--------

S. No.	Parameter	Value
1.	Oxide Thickness (T _{OX})	4 nm
2.	Physical Channel length (L _{ch})	45nm
3.	Power Supply	0.9 V
4.	Gate Dielectric	HfO ₂
5.	Dielectric Constant	16

S. No.	Parameter	CMOS-FC-OP AMP	PMOS-NCNT-FC-OP AMP	NMOS-PCNT-FC-OP AMP
1.	DC Gain in dB	32.3	36.8	45.7
2.	Average Power in uW	0.83	0.37	0.69
3.	Output Resistance in Ohm	363.7	339	126
4.	Bandwidth in MHz	1.46	1.12	0.64

Table 2: Comparative analysis of FC-OP AMPs with CL = 1 pf, VDD = 0.9V @ 45nm tech. node, N = 24, S = 20nm, D = 1.5nm.

IV. RESULTS AND DISCUSSION

In this research paper, simulation of innovative folded cascode Op Amp based on carbon nanotubes (CNT) has done at 45 nm . DC voltage gain, average power, bandwidth and output resistance have been computed using HSPICE Software. CNT based folded cascode Op Amp results in high performance with the increase of CNTs. Further, the simulation studies have revealed that the performance of the CNT based folded cascode Op Amp can be improved optimized at different CNTs.

REFERENCES

[1]. A.Javey et.al, (2004). "Self-Aligned ballistic molecular transistors and electrically parallel nanotube arrays", Nano Letters **4**: 1319–22.

[2]. J. O. Voorman, "Transconductance Op Amp," U.S. Patent 4 723 110, Feb. 2, 1988.

[3]. Tsung-Hsien Lin, Chin-Kung Wu, and Ming-Chung Tsai," A 0.8-V 0.25-mW Current-Mirror OTA With 160-MHz GBW in 0.18µm CMOS", *IEEE Transactions On Circuits And Systems—II: Express Briefs*, Vol. 54, No. 2, FEBRUARY 2007.

[4]. D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, H.S.P. Wong, Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications, *IEEE Transactions on Nanotechnology*, 7(5) (2008) 636–639.

[5]. A.K. Kureshi, M. Hasan, Comparison of performance of Carbon nanotube FET and bulk CMOS based 6T SRAM cell in deep submicron, *Microelectronics Journal*, **40**(6) (2009) 979–982.

[6]. T. Agarwal, A. Sawhney, A.K. Kureshi, M. Hasan, Performance comparison of CNFET and CMOS based full adders at the 32 nm technology node, Proceedings of VLSI Design and Test Symposium (VDAT) (2008) 49–57 Bangalore, India. [7]. R. Jacob Baker,"CMOS Circuit Design, Layout and Simulation" 3rd Edition, *IEEE Series on Microelectronic Systems*, page 797.

[8]. H.S. P. Wong, "Beyond the Conventional Transistor," *IBM Journal of Research & Development*, Vol. **46**, Issue 2.3, March 2002, pp. 133-168.

[9]. T. Skotnicki, J. A. Hutchby, T.J. King, H.S. P. Wong and F. Breuf, "The Road to the End of CMOS Scaling ", *IEEE Circuits Devices Magazine*, Vol. **21**, 2005, pp. 16 -26.

[10]. S. Iijima, and T. Ichihashi, Single-shell carbon nanotubes of 1-nm diameter, Nature (London), 1993, **363**, 603-605.

[11]. D.S. Bethune, C.H. Kiang, M.S. De Vries, G. Gorman, R. Savoy, J. Vazquez, and R. Beyers, Cobaltcatalysed growth of carbon nanotubes with singleatomic-layer walls, Nature (London), 1993, **363**, 605-607.

[12]. P. Avouris, "Supertubes: the Unique Properties of Carbon Nanotubes May Make Them the Natural Successor to Silicon Microelectronics," *IEEE Spectrum*, Vol. **41**, no. 8, August 2004, pp. 40-45.

[13]. <u>https://www.stanford.edu/group/nanoelectronics/</u> model_downloads. htm.

[14]. J. Deng and H.-S.P. Wong, "A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non idealities and Its Application -Part I: Model of the Intrinsic Channel Region," *IEEE Transactions on Electron Devices*, vol. **54**, 2007, pp. 3186-3194.

[15]. J. Deng and H.-S.P. Wong, "A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non idealities and Its Application- Part II: Full Device Model and Circuit Performance Benchmarking," *IEEE Transactions on Electron Devices*, Vol. 54, 2007, pp. 319-3205. [16]. A. Balijepalli, S. Sinha and Y. Cao, Compact modeling of carbon nanotube transistor for early stage process-design exploration, in: *Proceedings of the 2007 International Symposium on Low Power Electronics and Design, Portland, USA, Aug. 2007, pp. 2–7.*

[17]. A. Keshavarzi, A. Raychowdhury, J. Kurtin, K. Roy, Vivek De, Carbonnanotube field-effect transistors for high-performance digital circuits—transient analysis, parasitics, and scalability, *IEEE Transactions on Electron Devices* **53**(11)(2006).

[18]. H.P. Wong, David J. Frank, P. Solomon, C.J. Wann, J.J. Welser, Nanoscale CMOS, *IEEE Proceedings* 87(4) (1999).

[19]. A. Raychowdhury, K. Roy, Carbon nanotube electronics: design of high- performance and low power digital circuits, *IEEE Transactions on Circuits and Systems-I: Regular Papers* **54**(11) (2007).